

LeMeniz Technologies Private Limited

No.44, 100 feet road, Natesan Nagar
Pondicherry

Contact: +91 9962588976/9566475911

Websites: <https://www.lemenizinfotech.com/> / <https://ieeemaster.com/>

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S.No	IEEE 2021-2022 VLSI Project Titles	Domain	Year
1	Capacitive Modeling of Cylindrical Surrounding Double-Gate MOSFETs for Hybrid RF Applications	VLSI	2021
2	Dielectric-Modulated Bulk-Planar Junctionless Field-Effect Transistor for Biosensing Applications	VLSI	2021
3	Fast and Accurate Estimation of Statistical Eye Diagram for Nonlinear High-Speed Links	VLSI	2021
4	Cost-Effective Test Screening Method on 40-nm Embedded SRAMs for Low-Power MCUs	VLSI	2021
5	Reusable Delay Path Synthesis for Lightning Asynchronous Pipeline Controller	VLSI	2021
6	Novel Architecture for Lifting Discrete Wavelet Packet Transform With Arbitrary Tree Structure	VLSI	2021

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7	PWL-Based Architecture for the Logarithmic Computation of Floating-Point Numbers	VLSI	2021
8	Functional Constraints in the Selection of Two-Cycle Gate-Exhaustive Faults for Test Generation	VLSI	2021
9	An Efficient Parallel Processor for Dense Tensor Computation	VLSI	2021
10	A 13-bit 312.5-MS/s Pipelined SAR ADC With Open-Loop Integrator-Based Residue Amplifier and Gain-Stabilized Integration Time Generation	VLSI	2021
11	PhaseCamouflage: Leveraging Adiabatic Operation to Thwart Reverse Engineering	VLSI	2021
12	Cryptographic Accelerators for Digital Signature Based on Ed25519	VLSI	2021
13	A Three-Stage Comparator and Its Modified Version With Fast Speed and Low Kickback	VLSI	2021

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14	A 120–150 GHz Power Amplifier in 28-nm CMOS Achieving 21.9-dB Gain and 11.8-dBm Psat for Sub-THz Imaging System	VLSI	2021
15	A Bidirectional Nonlinearly Coupled QVCO With Passive Phase Interpolation for Multiphase Signals Generation	VLSI	2021
16	ASSURE: RTL Locking Against an Untrusted Foundry	VLSI	2021
17	Architectural Exploration for Energy-Efficient Fixed-Point Kalman Filter VLSI Design	VLSI	2021
18	Droplet Transportation in MEDA-Based Biochips: An Enhanced Technique for Intelligent Cross-Contamination Avoidance	VLSI	2021
19	Parallel and Flexible 5G LDPC Decoder Architecture Targeting FPGA	VLSI	2021
20	High-Performance Logic-on-Memory Monolithic 3-D IC Designs for Arm Cortex-A Processors	VLSI	2021
21	DOVA PRO: A Dynamic Overwriting Voltage Adjustment Technique for STT-MRAM L1 Cache Considering Dielectric Breakdown Effect	VLSI	2021
22	An Ultralow-Power OOK/BFSK/DBPSK Wake-Up Receiver Based on Injection-Locked Oscillator	VLSI	2021
23	Development of a Photoelectric Adjustment System With Extended Range for Fluorescence Immunochromatographic Assay Strip Readers	VLSI	2021

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Adding Technologies to Business

Software Development & Research Centre

24	AI-Powered Terahertz VLSI Testing Technology for Ensuring Hardware Security and Reliability	VLSI	2021
25	A Generalized Power Supply Induced Jitter Model Based on Power Supply Rejection Ratio Response	VLSI	2021
26	Enabling Write-Reduction Multiversion Scheme With Efficient Dual-Range Query Over NVRAM	VLSI	2021
27	Converter-Free Power Delivery Using Voltage Stacking for Near/Subthreshold Operation	VLSI	2021

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28	An Efficient VLSI Architecture for FastICA by Using the Algebraic Jacobi Method for EVD	VLSI	2021
29	A 3-Phase Resonant Switched-Capacitor Converter for Data Center 48-V Rack Power Distribution	VLSI	2021
30	On the Design of a Fault-Tolerant Scalable Three Dimensional NoC-Based Digital Neuromorphic System With On-Chip Learning	VLSI	2021
31	Splitter Trees in Single Flux Quantum Circuits	VLSI	2021
32	Analytical Modeling of Jitter in Bang-Bang CDR Circuits Featuring Phase Interpolation	VLSI	2021
33	ARXON: A Framework for Approximate Communication Over Photonic Networks-on-Chip	VLSI	2021
34	A 32-Gb/s PAM-4 SST Transmitter With Four-Tap FFE Using High-Impedance Driver in 28-nm FDSOI	VLSI	2021
35	Design of FPGA-Implemented Reed–Solomon Erasure Code (RS-EC) Decoders With Fault Detection and Location on User Memory	VLSI	2021
36	An Efficient 3D ReRAM Convolution Processor Design for Binarized Weight Networks	VLSI	2021
37	A 64.1mW Accurate Real-Time Visual Object Tracking Processor With Spatial Early Stopping on Siamese Network	VLSI	2021
38	A 43.1TOPS/W Energy-Efficient Absolute-Difference- Accumulation Operation Computing-In-Memory With Computation Reuse	VLSI	2021

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